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CLAIMS

What is claimed is:

1. An island photodiode comprising:

a core;

light sensing sidewalls along an exterior of said core; and

logic circuitry above said core.

2. The island photodiode in claim 1, wherein said sidewalls are perpendicular to a surface of said photodiode that receives incident light.

3. The island photodiode in claim 1, wherein said light sensing sidewalls comprise a junction region that causes electron transfer when struck with light.

4. The island photodiode in claim 1, wherein said logic circuitry blocks light from said core.

5. The island photodiode in claim 1, wherein said sidewalls comprise four vertical sidewalls.

6. The island photodiode in claim 1, wherein said core comprises a n+ core and said sidewalls comprise p+ sidewalls.

7. A photodiode array comprising:

a plurality of photodiode cores;

light sensing sidewalls along an exterior of said cores;

logic circuitry above said cores;

trenches separating said cores; and

a transparent material in said trenches.

8. The photodiode array pixel in claim 7, wherein said sidewalls are perpendicular to a surface of said photodiode that receives incident light.

9. The photodiode array in claim 7, wherein said light sensing sidewalls comprise a junction region that causes electron transfer when struck with light.

10. The photodiode array in claim 7, wherein said logic circuitry blocks light from said core.

11. The photodiode array in claim 7, wherein said sidewalls comprise four vertical sidewalls.

12. The photodiode array in claim 7, wherein said core comprises a n+ core and said sidewalls comprise p+ sidewalls.

13. A p-i-n island photodiode comprising:

a n+ core having a cube shape;

an intrinsic layer surrounding sides of said n+ core;

a p+ layer surrounding sides of said intrinsic layer; and

at least one transistor above said n+ core.

14. The p-i-n island photodiode in claim 13, further comprising an n-well between and connecting said n+ core and said transistor.

15. The p-i-n island photodiode in claim 13, wherein said p+ layer comprises a p-type doped layer having a doping concentration in the range from 1e15 to 1e18 cm^3.

16. The p-i-n island photodiode in claim 13, wherein n+ core comprises an n-type doped layer having a doping concentration in the range from 10e15 to 10e17 cm^3.

17. The p-i-n photo diode in claim 13, further comprising an anti-reflective coating surrounding sides of said p+ layer.

18. The p-i-n photo diode in claim 13, further comprising a transparent material adjacent said anti-reflective coating.

19. The p-i-n photo diode in claim 18, further comprising wiring levels above said transistor and said transparent regions, wherein said wiring levels include transparent regions above said transparent material.

20. A method of forming an island photodiode comprising:

forming a core in a substrate;

forming trenches in said substrate adjacent said core;

forming light sensing sidewalls along said trenches; and

forming logic circuitry above said core.

21. The method in claim 20, wherein said sidewalls are perpendicular to a surface of said photodiode that receives incident light.

22. The method in claim 20, wherein said forming of said light sensing sidewalls comprises doping sidewalls of said trench to form a junction region between said sidewalls and said core that causes electron transfer when said sensing sidewalls are struck with light.

23. The method in claim 20, wherein said logic circuitry blocks light from said core.

24. The method in claim 20, wherein said forming of said trenches forms four vertical sidewalls around said core.

25. The method in claim 20, further comprising doping said core with impurities to form an n+ core and doping said sidewalls with impurities to form p+ sidewalls.

26. A method of forming an array of island photodiodes comprising:

forming cores in a substrate;

forming trenches in said substrate adjacent said cores;

forming light sensing sidewalls along said trenches; and

forming logic circuitry above each of said cores.

27. The method in claim 26, wherein said sidewalls are perpendicular to a surface of said photodiode that receives incident light.

28. The method in claim 26, wherein said forming of said light sensing sidewalls comprises doping sidewalls of said trench to form a junction region between said sidewalls and said cores that causes electron transfer when said sensing sidewalls are struck with light.

29. The method in claim 26, wherein said logic circuitry blocks light from said cores.

30. The method in claim 26, wherein said forming of said trenches forms four vertical sidewalls around each of said cores.

31. The method in claim 26, further comprising doping said cores with impurities to form an n+ core and doping said sidewalls with impurities to form p+ sidewalls.